BROADCOM 802.11AX Solution:BCM4908+BCM43684

Broadcom 11AX Structure:

BROADCOM 11AX Solution:BCM4908+BCM43684*3

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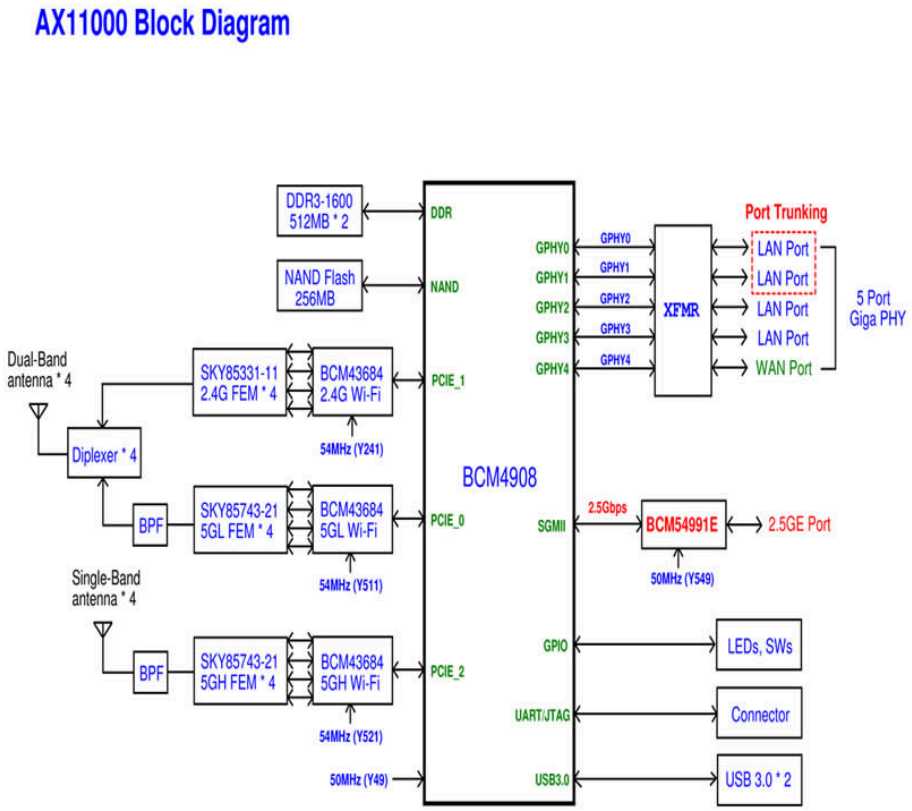
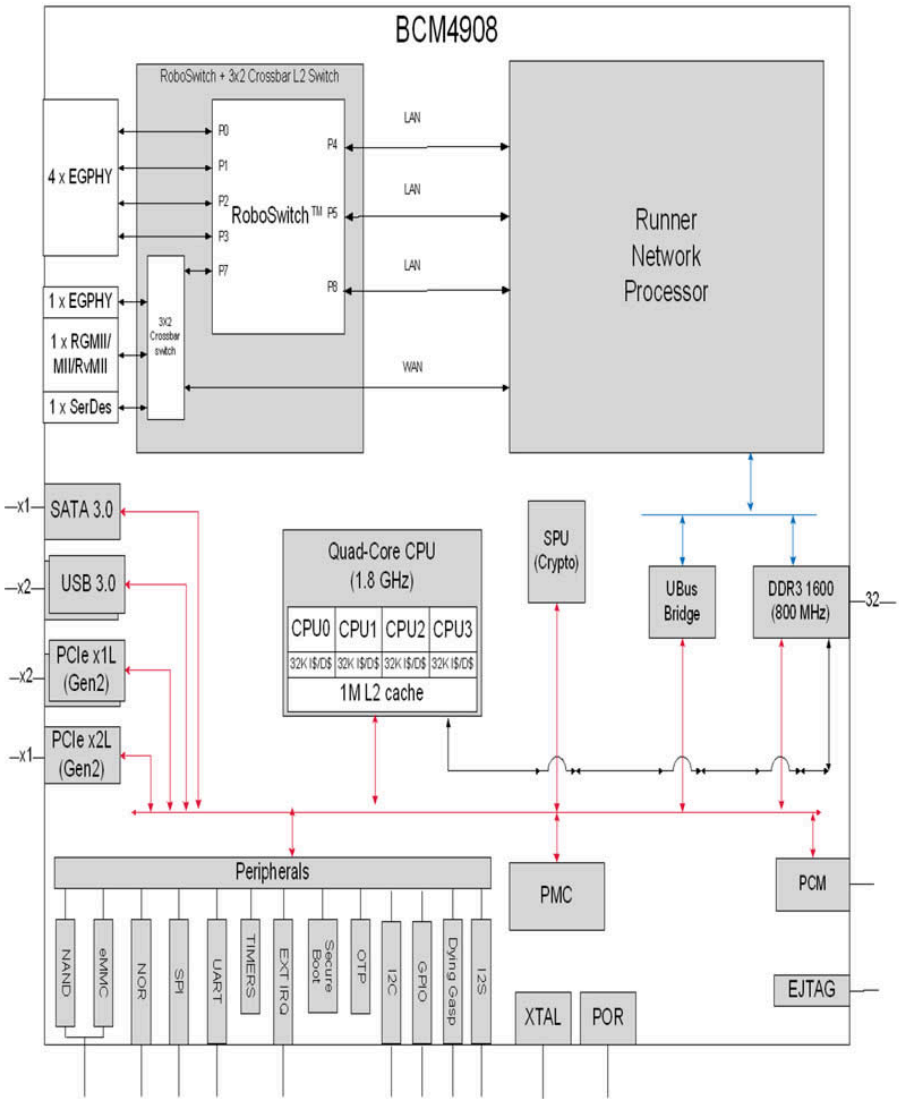


BCM4908 Functional block diagram



BCM4908

Quad-Core Wi-Fi Communications Processor

GENERAL DESCRIPTION FEATURES

The BCM4908 is a high-performance, nextgeneration communications processor that enables feature-rich, low-cost low power, multigigabit Wi-Fi residential routers, service provider gateways, or enterprise access points.

Feature Summary

System Processor

• 1.8 GHz quad-core ARMv8 compatible processor core
– 32K I-cache and 32K D-cache per core
– 1 MB shared L2 cache

External Interfaces

• DDR
– 800 MHz, 32-bit DDR3 (1600 MHz)
– Supports up to 2 GB devices
– Built-in reference voltage for 1.5V nominal voltage (DDR3) and 1.35V low voltage (DDR3L) modes
• Single 50 MHz reference crystal or oscillator
• Two single-lane PCIe 2.0 Gen 1 or Gen 2 and one dual-lane PCIe 2.0 Gen1 or Gen2 speed interfaces to support concurrent 802.11 wireless networking
• Four gigabit Ethernet PHY ports (GPHY0, GPHY1, GPHY2, and GPHY3)
• Two configurable p orts —Select from the following three ports to configure one as a LAN port and one as a WAN port: RGMII/MII/RvMII, GPHY4, and 10/100/1000/2500 Mbps Ethernet SerDes

• USB
– Two USB ports configurable as either USB 3.0 host or USB 2.0 host
– USB host controller specification 3.0 supporting up to two root hub ports
– USB revision 3.0/2.0/1.1 compatible
– SuperSpeed eXtensive HC Interface (xHCI) 1.0 compatible
– Enhanced-HCI revision 1.0 compatible
– Open-HCI revision 1.0a compatible
– Integrated MAC and transceiver (with internal terminations)

• SATA
– SATA III 6 Gbps interface
– eSATA support, 3 Gbps interface
– AHCI 1.3 specifications compliant port
– Supports specs: Gen1m, Gen1i, Gen2i, Gen2m, Gen3l
– Supports full 5500 ppm SSC on received data

• PCM highway
– Eight-channel TDM (PCM highway) controller with integrated transmit/receive DMA for each channel
– DMA and programmed IO support
– Falling-edge frame sync trigger, frame sync duration control

– Data sampling offset control, time slot select
– Programmable data format: 8-bit or 16-bit data
– TDM master and slave operation

• Miscellaneous peripheral support
– Two UARTs
– External interrupt-configurable on any GPIO pins
– I2S
– High-speed SPI master interface with up to six chip selects, operating up to 100 MHz (programmable)
– NAND Flash interface
– Can boot from NAND and SPI-NAND initially, and eMMC later
– Timer/counters
– Watchdog timer
– Interrupt control

• Network timing reference (NTR)
Gigabit Ethernet Switch

• Multiple switch ports support
– Four 10/100/1000 LAN ports to/from four integrated auto-MDIX 10/100/1000BASE-T transceivers with EEE support
– One configurable LAN port that can support one of the following: RGMII/MII/RvMII, GPHY, or 10/100/ 1000/2500 Mbps Ethernet SerDes (Configurable WAN and LAN port cannot be configured to support the same interface.)

• Supported features:
– QoS: IEEE 802.1p, IPv4/IPv6, MAC, Port and DiffServ based
– Port-based VLAN
– Port-based rate control
– Port mirroring
– IGMP snooping
– Double tagging (for ISP)
– IEEE 802.3x programmable per-port flow control and backpressure, with IEEE 802.1x support for secure user authentication
– Per-port MIB counters
– 4K entry MAC address table with automatic learning

and aging
– 384 KB packet buffer
– 128 multicast group support

• Ethernet 10/100/1000 transceivers
– 1000BASE-T (IEEE 802.3ab), 100BASE-TX (IEEE 802.3u), and 10BASE-T (IEEE 802.3) compliant
– Full-duplex or half-duplex Ethernet
– Auto-MDIX support
– 802.3az Energy Efficient Ethernet DMA Engines

• IUDMA
– PCM DMA
– USB DMA
Security Processing Unit

• Scalable bulk processing engine to support generic data encryption/decryption and hash authentication for a variety of algorithms, cipher modes, and operation orders

• The cryptographic processing capability of SPU includes:
– Cross-connected encryption and hash engines to support single pass AUTH-ENC or ENC-AUTH processing
– Scalable AES module to support CBC, ECB, CTR, CFB, OFB, XTS encryption with 128-bit, 192-bit, and 256-bit AES key sizes
– Scalable DES module to support DES and 3DES in ECB and CBC modes
– RC4 stream cipher module to support state initialization, state update, and key stream generation
– MD5/SHA1/SHA224/SHA256/SHA384/SHA512 combo engine to support pure hash or HMAC operations

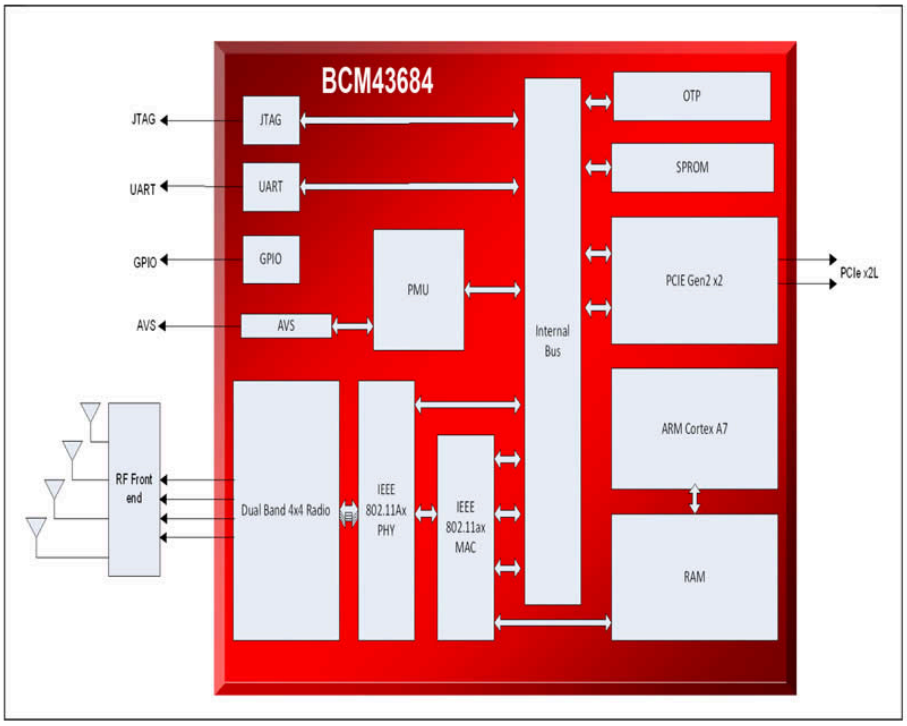
• Built-in 1 KB key cache for local protected key storage
Advanced Power Management

• Hardware sleep mode for wake from real-time counter or interrupt

• Advance power control of all on-chip modules

BCM43684 Functional block diagram

Figure 1: Functional Block Diagram



BCM43684

IEEE 802.11ax 4x4 2.4/5 GHz Single-Chip MAC/PHY/Radio

GENERAL DESCRIPTION FEATURES

The Broadcom BCM43684 is a dual-band (2.4 GHz and 5 GHz) 4×4 IEEE 802.11ax MAC/PHY/Radio System-on-a-Chip (SoC). The device enables the development of advanced high-efficiency wireless (HE) 802.11ax Access points, repeaters, and WLAN client solutions.

Features

• IEEE 802.11ax compliant.
• Dual-Band OFDMA allows for a higher density of simultaneous users.
• Quad-stream spatial multiplexing to 4.8 Gbps data rate.
• IEEE 802.11a/b/g/n/ax, 4×4 160 MHz channels.
• 1024-QAM modulation rates.
• 4×4 MU-MIMO on 80 MHz channels.
• Expanded 5 GHz frequency coverage including spectrum up to 5925 MHz expected to become available under new regulatory rules.
• Supports RangeBoost technology.
• Support for LDPC in both TX and RX for increased wireless coverage.
• 3+1 DSP-based Spectrum Capture and Zero Wait DFS.
• CQI and CSI can be captured and passed to the Host along with the MAC address associated with the captured data.
• Supports Digital Pre-Distortion (DPD) which reduces power consumption and improves Band Edge performance.
• Full IEEE 802.11a/b/g/n/ac legacy compatibility with enhanced performance.
• Complies with PCI Express base specification revision 2.0 for ×2 lane and power management base specification.
• Supports Linux for access point and router applications.
• Comprehensive wireless network security support that includes WPA, WPA2, and AES encryption/ decryption.
• Supports full-host CPU IEEE 802.11 packet offload.
• Available in a 13 mm × 13 mm, 284-pin 0.65 mm pitch (FCBGA) package.

Applications

• High-performance IEEE 802.11ax access points, routers, and home residential gateways.

Service Routers.